ABSTRACT OF THE DISCLOSURE

Methods and compositions are provided for planarizing a substrate surface with reduced or minimal topographical defect formation during a polishing process for dielectric materials. In one aspect a method is provided for polishing a substrate containing two or more dielectric layers, such as silicon oxide, silicon nitride, silicon oxynitride, with at least one processing step using a fixed-abrasive polishing article as a polishing article. The processing steps may be used to remove all, substantially all, or a portion of the one or more dielectric layers, which may include removal of the topography, the bulk dielectric, or residual dielectric material of a dielectric layer in two or more steps.

C:\NrPortbl\iManage\TTHOMAS\229386_1.DOC